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						P8900		10/774,990	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT						Applicant(s)			
(Use several sheets if necessary)						Matthew J. Amatangelo, et al.			
						Filing Date		Group	
						February 9, 2004		2123	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA								
	AB								
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	AK								
Foreign Patent Documents									
		Document	Date	Country	Class	Subclass	Translation		
							Yes	No	
	AL						<input type="checkbox"/>	<input type="checkbox"/>	
	AM						<input type="checkbox"/>	<input type="checkbox"/>	
	AN						<input type="checkbox"/>	<input type="checkbox"/>	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
8	AO	David Van Campenhout, Trevor Mudge, Kar�m A. Sakallah "Timing Verification of Sequential Domino Circuits," <i>Proc. TechCon 96</i> , September 1996							
8	AP	Pawan Kulshreshtha, Robert Palermo, Mohammad Mortazavi, Cyrus Bamji, Hakan Yalcin "Transistor-Level Timing Analysis Using Embedded Simulation" Cadence Design Systems, Inc. <a href="http://www.sigda.org/Archives/ProceedingArchives/iccad/iccad2000/papers/2000/iccad00/pdf/08a_3.pdf">www.sigda.org/Archives/ProceedingArchives/iccad/iccad2000/papers/2000/iccad00/pdf/08a_3.pdf</a>							
8	AR	Sumant Ramprasad, Ibrahim N. Hajj, Farid N. Najm "An Optimization Technique for Dual-Output Domino Logic," <i>Proceedings 1999 International Symposium on Low Power Electronics and Design</i> , p.258-260, August 16-17, 1999, San Diego, California							
	AS								
	AT								
Examiner <u>Shamlihan Patel</u>				Date Considered <u>1/30/07</u>					
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